CLAIMS:

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1. A semiconductor integrated circuit, comprising:

storing means that enables reading and writing;

comparing means that compare write data supplied to the storing means with data read from the storing means; and

variable address converting means that convert an address signal supplied to the storing means based on a comparison result in the comparing means, wherein an input signal of a logic circuit having a desired logical function is input as the address signal to the storing means, and wherein the data is written to the storing means so that the read data of the storing means can be obtained as an expected output signal with respect to the input signal of the logic circuit.

2. A semiconductor integrated circuit according to claim 1, wherein a plurality of the storing means, a plurality of the comparing means, and a plurality of the variable address converting means are provided on a single semiconductor chip.

3. A semiconductor integrated circuit according to claim 1 or 2, wherein the storing means are a volatile memory.

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4. A semiconductor integrated circuit according to claim 1, 2, or 3, wherein the variable address converting means comprise: a memory array in which a plurality of memory cells

are arranged in a matrix shape; an address decoder that selects the memory cells in the memory array based on an input address signal; reading means that amplify a signal read from the memory array; and operating means that update the input address signal based on a control signal.

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5. A semiconductor integrated circuit according to claim 4, wherein the memory array has the volatile memory.

6. A semiconductor integrated circuit according to claim 1, 2, 3, 4, or 5, further comprising: data holding means that can hold the data read from the storing means; a switch matrix that switches the input address signal or an output signal of the data holding means and can supply it to the variable address converting means; and the storing means that store the control information of each switch in the switch matrix.

7. A semiconductor integrated circuit according to claim 6, wherein the data holding means comprise: latching means that can latch first data read from the memory circuit; and gate means that permit or do not permit latching of the first data to the latching means based on the first data read from the memory circuit.

8. A method for constructing a logic integrated circuit,

wherein the logic integrated circuit having a desired logical function is constructed by decoding design data of a function level described in HDL by control means using the semiconductor integrated circuit according to claim 1, 2, 3, 4, 5, 6, or 7 and assigning to the self-construction circuit a signal that decides a logical configuration of a self-construction circuit capable of constructing optional logic from the control means.

9. A method for constructing the logic integrated circuit according to claim 8, wherein the control means are formed on the same semiconductor chip as the self-construction circuit.

10. A method for constructing the logic integrated circuit according to claim 9, wherein a storage that stores the design data of the function level are formed on the same semiconductor chip as the control means and the self-construction circuit.

11. A semiconductor integrated circuit, comprising storing means that hold information obtained from a description in which a logical function is represented in hardware description language and obtain the output of the logical function that complies with an input signal from the output terminal, using the signal supplied to the address terminal as the input signal.

12. A semiconductor integrated circuit according to claim 11, wherein the logical function includes a combinational logical function.

13. A semiconductor integrated circuit according to claim 12, wherein the logical function includes a sequential logical function.

14. A semiconductor integrated circuit according to claim 11, wherein the storing means are read- and write-enable storing means.

15. A semiconductor integrated circuit according to claim 11, wherein converting means that form the information written to the storing means from the description represented in the hardware description language and the storing means are formed on the same semiconductor chip.

16. A semiconductor integrated circuit according to claim 15, wherein the storing means that hold the description represented in the hardware description language are formed on the semiconductor chip.

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